A High-Yield, 3–7-GHz, 0.5-W Push-Pull GaAs MMIC Amplifier

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Abstract—**A high-yield, 3–7-GHz, 0.5-W MMIC GaAs amplifier has been successfully designed and tested. The amplifier features small chip size (1.2 mm sq.), high gain (12 ± 1.5 dB), high power-added efficiency (20 percent), good RF yield (57 percent), and high tolerance to process variations. Packaged amplifiers were built with this chip for both the 2–6-GHz and the 5.9–6.4-GHz bands. Saturated output power of 25 dBm was achieved in the 2–6-GHz band, and 27 dBm in the 5.9–6.4-GHz band. Infrared measurements show that the device has low FET channel temperatures when operated at full bias power over the full range of military ambient temperatures.**

I. Introduction

SIGNIFICANT PROGRESS in the design of GaAs monolithic amplifiers has occurred over the last several years. Impressive power out per FET periphery, high efficiencies, and multioctave bandwidths have been reported [1]. Most of the previously reported designs, however, have used a relatively large chip area and have utilized such techniques as excessively thin chips, selective back etching, via hole grounds, or wraparound grounds [2]–[5].

These special processing steps are not only expensive in themselves, but reduce wafer yields. The end result is that the solid-state amplifier represents a disproportionate part of the cost of any microwave system. The increasing need for MMIC power amplifiers in disposable military systems and for low-cost communication systems mandates a reduction in the cost of the power amplifiers.

In this paper, we describe a medium-power 3–7-GHz amplifier designed to maximize performance for the highest yield. Improvements made in the electrical design, the MMIC layout, and the processing technology to achieve these goals are discussed.

II. Circuit Description

Fig. 1 shows the schematic of a two-stage MESFET amplifier with 4-mm output gate periphery, and 6 mm overall. The circuit integrates all matching, biasing, bypassing, and coupling components. Matching sections were designed with minimal series inductances to minimize the circuit losses.

The amplifier uses a novel bias scheme that requires only a single drain supply. The scheme uses a source bias resistor that allows a constant I_{DS} independent of I_{DSS}. Hence, no gate bias correction is needed to achieve the proper FET bias point, and the amplifier requires only a single supply. Note that biasing an implanted FET at a constant I_{DS} independent of I_{DSS} also stabilizes the FET reactances—C_{gs} in particular—which, in turn, improves RF yields.

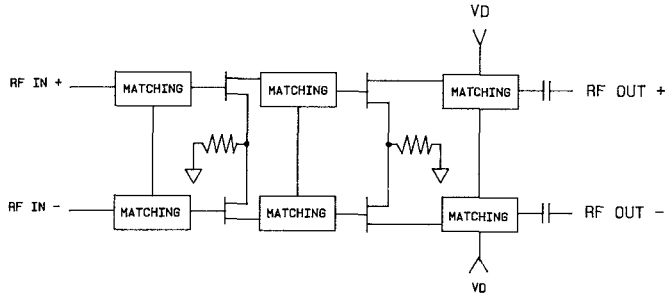

Fig. 1. Schematic of 3–7-GHz power MMIC amplifier.

The amplifier utilizes a push-pull configuration. This allows the doubling of the output power capability. It also provides for low source impedance and minimum second-harmonic distortion.

III. Processing Technology

The goals in selecting a processing technology were to avoid processing techniques that increase cost and decrease yields, and yet not sacrifice performance. The GaAs power MMIC was manufactured using an ion-implanted MESFET process. The virtual ground of the balanced (push-pull) design removes the need for plated-through holes (vias). In addition, wafer thinning was not required to establish a ground plane in close proximity to the circuitry. Chip thickness was determined primarily by thermal considerations. The thickness was selected to be 0.2 mm, which was sufficient to maintain proper channel temperature under normal operating conditions and yet thick enough to prevent most wafer breakage. The thickness of the chip was sufficient to minimize the effects of capacitances to ground through the chip.

Well-characterized 1-μm FET's were utilized for this design. First metal and air-bridge metallizations were used for interconnections. SiN MIM's provided dc blocking and matching capacitors.

IV. Layout

A photomicrograph of the MMIC amplifier is shown in Fig. 2. For cost reasons, the amplifier layout was made as compact as possible without sacrificing the chip thermal

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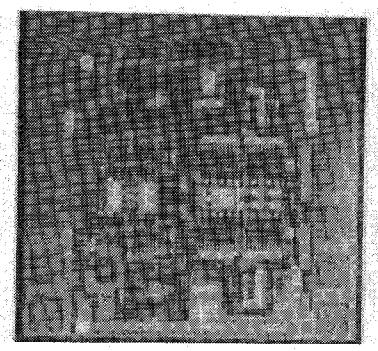


Fig. 2. 3–7-GHz MMIC amplifier chip photograph.

design. The use of all lumped matching elements facilitated the design compaction. The balanced two-stage amplifier required a 1.2-mm-sq. chip area. With this chip size, 3200 MMIC amplifiers can be obtained on a single 3-in-diameter wafer.

For thermal considerations, all heat sources were spread evenly about the chip. The FET's were broken up into 1-mm periphery sections, and then separated at their centers to avoid the central hot spots associated with large periphery power amplifiers. The bias resistors were similarly broken up and spread throughout the chip.

Note that power amplifier circuits with their large FET peripheries are particularly sensitive to parasitic source inductances. Very low source inductances can be achieved by the use of a virtual ground, as in a push-pull amplifier. This reduction in source inductance makes the amplifier less sensitive to C_{gs} variations, thereby improving RF yields.

V. MMIC Results

The performance of the amplifier was first measured at wafer level. Fig. 3 is a plot of the small-signal gain response of the device. The power amplifier demonstrated 12 ± 1.5 dB gain across the 3–7-GHz band. Fig. 4 is a small-signal gain plot of all the amplifiers that exhibited a minimum of 10 dB gain. Of the 40 chips on the wafer randomly selected for testing, 23 had at least 10-dB gain, for a yield of 57 percent. For 8-dB minimum gain, the yield would have been 77 percent. All but four devices turned on, for a dc yield of 90 percent.

Fig. 5 shows the power saturation characteristics of the amplifier. Saturated power output of 550 mW was achieved across the 3–5.5-GHz band, with an associated gain of 9.5 dB. At this power level, the amplifier dissipates 2.5 W, resulting in an overall power-added efficiency of 20 percent.

Since the cost of a device is directly related to chip size, a good figure of merit for production MMIC amplifiers is P/A, power output per unit chip area. In Fig. 6, we have compared the power output per chip area of the 3–7-GHz power amplifier with many of the previously published power MMIC amplifiers [1]. The 3–7-GHz amplifier

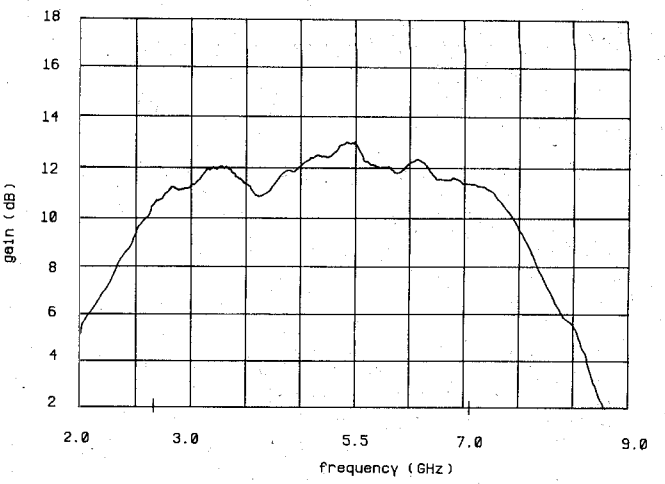


Fig. 3. Small-signal gain versus frequency of 3–7-GHz MMIC amplifier.

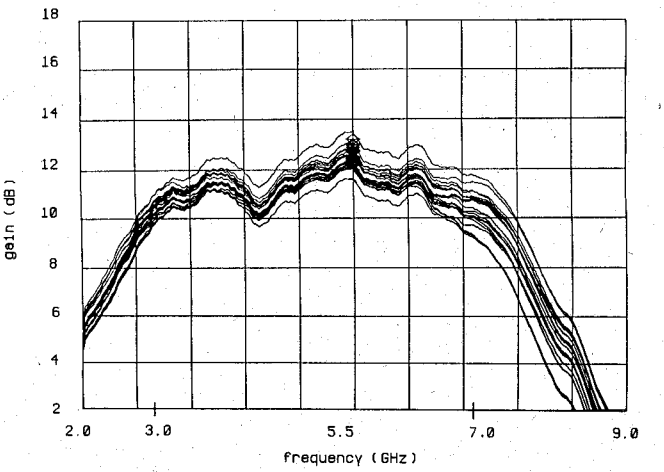


Fig. 4. Variation in gain across wafer for 3–7-GHz MMIC amplifier.

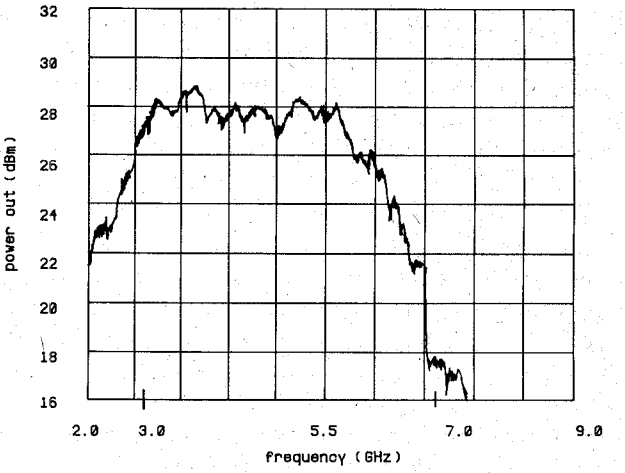


Fig. 5. Saturated power output of 3–7-GHz MMIC amplifier.

exhibited 0.45 W/mm sq. This, to our knowledge, is the largest power out per chip area reported to date.

Fig. 7 plots another figure of merit, G/A, gain/mm sq., for these power amplifiers. The 3–7-GHz amplifier had the best reported G/A of 8 dB/mm sq.

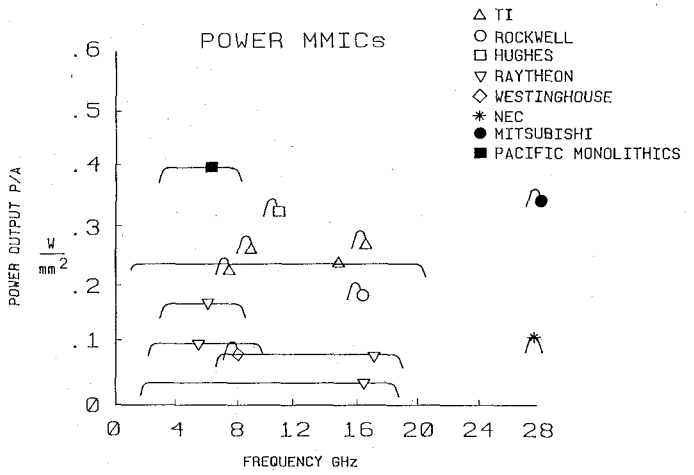


Fig. 6. Power output per chip area of published power amplifier.

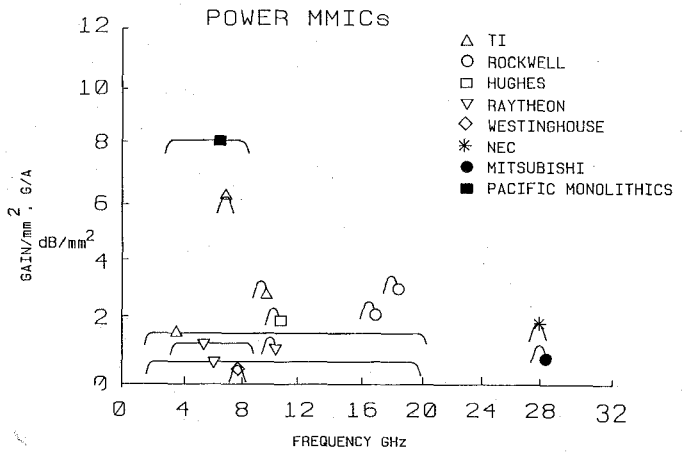
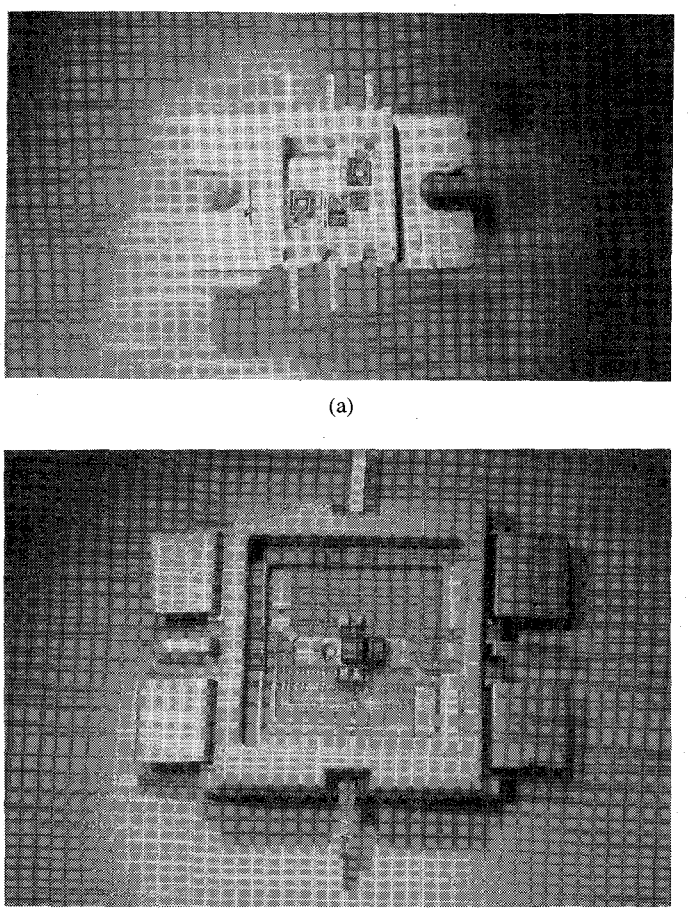


Fig. 7. Gain per chip area of published power amplifier.



(a) (b)

Fig. 8. (a) Two-chip power amplifier in six-lead package. (b) Two-chip power amplifier in four-lead package.

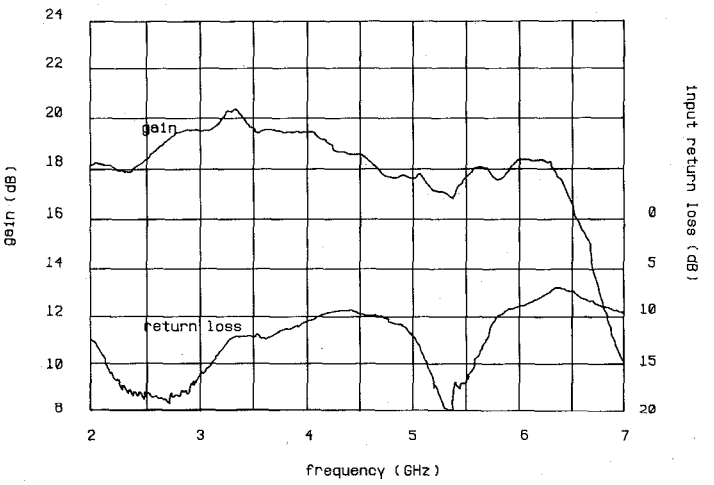


Fig. 9. Small-signal response of 2–6-GHz packaged amplifier.

VI. Packaged MMIC Results

The 0.5-W power chip was combined with a 2–6-GHz small-signal MMIC amplifier to produce a 2–6-GHz, 18-dB gain power amplifier. The low-power amplifier was a two-stage, push-pull device. It was used to increase the gain of the overall amplifier and to improve the combined amplifier gain bandwidth down to 2 GHz. The combined amplifier also had improved input return loss.

The amplifier was placed in various packages, along with MIC baluns to interface to single-ended test equipment. Fig. 8(a) shows the amplifier along with two discrete MIC baluns in a six-lead package. Fig. 8(b) shows the device on a dual-balun BeO substrate in a four-lead package. Either one of these packages can be used to build multistage amplifiers. Both packages provided better than 15-dB return loss up to 8 GHz. Feedback capacitances were kept to a minimum by making the package side walls much higher than the combined MMIC and MIC. Isolation between leads was not an issue in the four-lead package and was minimized in the six-lead package by side wall grounds between the leads.

The small-signal response of the six-lead package amplifier is shown in Fig. 9.

The same device was then inductively tuned using 1-mil bond wires to produce a 0.5-W, 5.9–6.4-GHz amplifier. The amplifier had a small-signal gain of 18 dB (Fig. 10). Its saturated response is shown in Fig. 11.

The thermal resistance of the MMIC power amplifier on a BeO substrate was measured with an infrared radiometric microscope. The 0.2-mm chip operating at 2.5-W dissipation had a measured thermal resistance of 10°C/W.

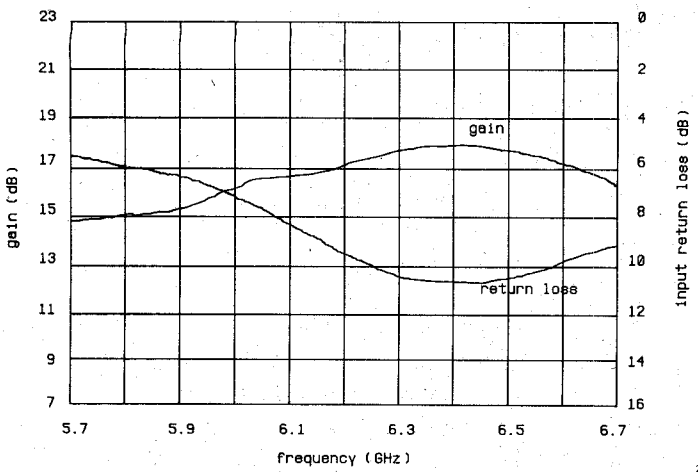


Fig. 10. Small-signal response of 5.9–6.4-GHz packaged amplifier.

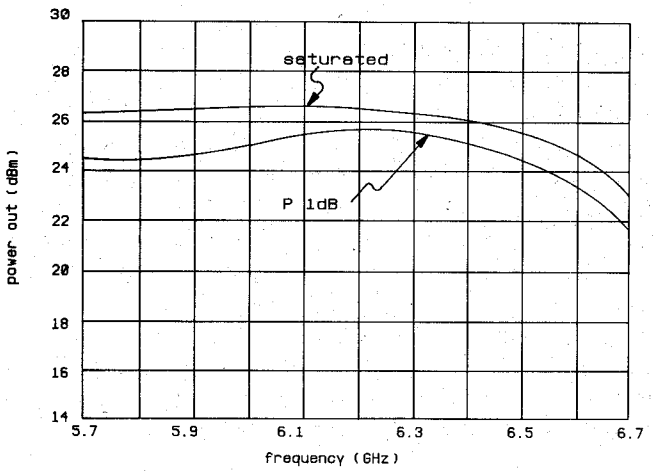


Fig. 11. Saturated response of 5.9–6.4-GHz packaged amplifier.

This would correspond to a 25°C rise in FET channel temperature from ambient. Assuming a heat sink temperature of even 125°C would give a channel temperature of only 150°C. The projected MTTF for such a device would then be 2 million hours [7].

This low thermal resistance is due to the effort made in spreading the heat sources throughout the die area. The infrared measurements showed that although there were a few hot spots, the thermal flux was well spread out across the surface of the device. Note also that the 0.2-mm thickness of the die was selected for both ease of handling and thermal considerations.

VII. Conclusions

GaAs monolithic power amplifiers are entering the age of high RF yields and low-cost chips. By using process tolerance design and by paying close attention to processing costs and yield enhancement factors, we developed a 3–7-GHz medium-power MMIC amplifier with net yields close to 60 percent on 3-in wafers with 3200 possible chips per wafer. The MMIC amplifier was used to make a 2–6-GHz and a 5.9–6.4-GHz packaged amplifier. Both amplifiers typically had 18-dB gain. The narrow-band amplifier exhibited a 27-dBm power output.

The MMIC on a BeO substrate had a junction temperature rise of no more than 25°C from ambient. MTTF for the device on heat sinks at normal military temperatures is in the order of millions of hours.

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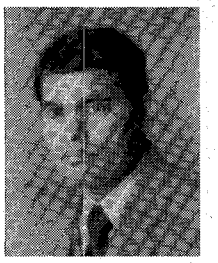

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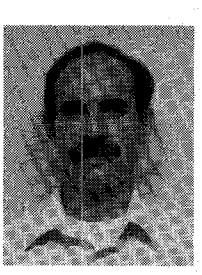

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